Amendments to the Specification

Please amend the specification as follows:

[0011] Another embodiment of the invention relates to a method of forming a transistor having a gate width of less than 70 nm. The method includes E-beam ~~radiation~~ irradiation of a gate pattern of a photoresist layer, and trimming the E-beam ~~eradiated~~ irradiated gate pattern of the photoresist layer. The method further includes etching a polysilicon layer disposed below the photoresist layer in accordance with the trimmed gate pattern to form a gate of the transistor. The gate width is preferably less than 70 nm.

[0012] Still another embodiment of the invention relates to an integrated circuit. The integrated circuit includes an isolation region and a transistor surrounded by the isolation region. The transistor includes a gate. A critical dimension of the gate is less than approximately 60 nm. The gate is defined by an E-beam ~~eradiated~~ irradiated gate feature on a photoresist layer and trimming the E-beam radiation ~~eradiated~~ irradiated gate pattern of the photoresist layer, while preserving the gate to isolation line extension to ensure enhanced transistor performance.

[0033] After developing step 10, but before first and second features 26, 36 are transferred onto any of the underlying layer(s) (layers 40 and 42 are etched), wafer 20 containing a pattern (resist features 26, 36) is exposed to a precisely controlled flood electron beam exposure (E-beam ~~radiation~~ irradiation step 12). The flood electron beam impinges and penetrates the exposed first and second features 26, 36 and chemically modifies or transforms ~~E-beam radiation~~ such exposed structures to affect the etch characteristics of first and second features 26, 36. In particular, a horizontal or trim etch rate, a vertical or erosion etch rate, and an erosion rate of a minimum extension onto isolation regions 30 of each of first and second features 26, 36 are affected to facilitate and control etching of first and second features 26, 36 in resist trimming step 14.

[0035] The electron beam flood exposure conditions or parameters (e.g., dose, accelerating voltage, and beam current) are selected to provide optimum desirable etch trimmability and etch stability characteristics to first and second features 26, 36 for resist trimming step 14. The electron beam exposure E-beam ~~radiation~~ irradiation conditions can

vary depending on the type of photoresist material, subsequent processing steps involving the E-beam ~~eradiated~~ irradiated photoresist, and/or desired characteristics of the photoresist material. An exemplary electron-beam cure recipe delivers a total electron dose (e.g., 2000uC/cm2) in one or more steps having accelerating voltages from 50 to 2000V depending on the resist and application.

[0036] The photoresist material comprising first and second features 26, 36 is a 248 nm photoresist material (e.g., a polystyrene-based polymer) which typically exhibits a higher ratio of vertical to horizontal resist consumption rates, so substantial process latitude is present without the use of ~~an~~ E-beam ~~radiation~~ irradiation. The higher e-beam ~~radiation~~ irradiation doses are required to obtain adequate e-beam induced cross linking of the polymer in order to realize the desirable trim etch enhancements. The acrylate and alicyclic-based resists have higher e-beam induced cross-linking efficiency. Thus, it is expected to require a ~~HIGHER~~ higher dose at a given energy to achieve the same result in a 248 nm resist.

[0037] E-beam ~~radiation~~ irradiation step 12 imparts a chemical change, i.e., cross-linking and decomposition, to the functional groups and additives in the regions of the photoresist material which are bombarded by the electron beam. Such regions of the photoresist material will accordingly have increased etch resistance (i.e., reduced etch rate), bulk modulus, bulk toughness, and interfacial toughness of the substrate-resist polymer bond (i.e., the bond between the photoresist layer and ARC layer 42). The cross-linked or e-beam ~~eradiated~~ irradiated regions can be the top portion, the top and side portions, or the entire feature of each of first and second features 26, 36. An exemplary electron-beam cure recipe delivers a total electron dose (e.g., 2000uC/cm2) in one or more steps having accelerating voltages from 50 to 2000V depending on the resist and application.

[0038] The extent to which first and second features 26, 36 should be e-beam ~~eradiated~~ irradiated (e.g., the e-beam ~~eradiated~~ irradiated depth, E-beam ~~eradiated~~ irradiated region(s), and degree of decomposition of the functional groups of the photoresist material) depends on, among others, the extent to which the E-beam ~~eradiated~~ irradiated first and second features 26, 36 are trimmed in trimming step 14. The E-beam ~~eradiated~~ irradiated or penetration depth and E-beam ~~eradiated~~ irradiated region(s) of first and second features 26, 36 are related to the electron beam flood exposure conditions, processing gas(es), and or wafer

temperature. The degree of decomposition of the functional groups of the photoresist material is related to the total electron dose electrons per unit area as well as to the doses and energies of the individual steps in the E-beam ~~radiation~~ irradiation recipe sequence. There may be a dependence on substrate temperature as well.

[0039] After E-beam ~~radiation~~ irradiation step 12, wafer 20 undergoes resist trimming step 14. Trimming step 14 is preferably a plasma etching step. Wafer 20 is exposed to a plasma etchant to trim or reduce the dimensions of features patterned on the photoresist layer, such as, first and second features 26, 36. The plasma etchant can comprise a variety of plasma etch chemistries, such as, O_2, HBr/O_2, Cl_2/O_2, $N_2/He/O_2$, or N_2/O_2. A variety of standard etching equipment, such as those manufactured by Applied Materials of Santa Clara, California, or Lam Research of Freemont, California, may be utilized to provide the plasma etchant. An exemplary trim/gate stack etch can employ HBr/O2/Ar chemistry for the resist trim, CF4/Ar chemistry for the ARC etch, and a sequence of steps employing one or more of HBr, HeO2, CF3, and CI2 for the ~~poly-silicon~~ polysilicon etch.

[0040] The plasma etchant etches all exposed surfaces between first and second features 26, 36, including the top and side surfaces, to form first and second trimmed gate features 28, 38, respectively (shown in dotted lines in FIGs. 2-4). Because different regions or portions of each of first and second features 26, 36 have different etch rates relative to each other following E-beam ~~radiation~~ irradiation step 12 (e.g., vertical etch rate vs. horizontal etch rate), the dimensional reduction of all of the surfaces of first and second features 26, 36 is not the same.

[0044] Preferably, first and second gates 70, 74 have gate widths comparable to width 60. First gate 70 includes a minimum extension 72 onto isolation regions 30 and second gate 74 includes a minimum extension 76 onto isolation regions 30. Each of minimum extensions 72, 76 has a length comparable to extended length 62. The width along the length of each of first and second gates 70, 74 has a variation of less than 1 nm, as opposed to a gate formed from photoresist that was not e-beam ~~eradiated~~ irradiated which has a gate width variation along its length of approximately 5 nm. In one embodiment, the local gate width variation is between 4 to 6 nm over a 3 nm gate length (3 sigma). Preferably this variation can be further reduced as technology permits.

[0045] In this manner, transistors having narrow and uniform gate widths can be consistently fabricated. Because there is less consumption of the minimum extension of each gate onto the field isolation region (i.e., reduced rate of end-cap pull back during the resist trimming process), an increased number of transistors can be provided per unit area and the number of defective transistors is decreased. E-beam ~~radiation~~ irradiation the gate feature patterned on the wafer with an electron beam after development but before the resist trimming process imparts desirable etch characteristics to such patterned features and even to photoresist materials that have inherently poor trim properties. Accordingly, after the E-beam ~~eradiated~~ irradiated gate features have been trimmed, the trimmed gate features enjoy several advantages, including higher uniformity in the gate widths or critical dimensions between gates, higher uniformity in the gate width or critical dimension along the length of a given gate, a narrower gate width, a reduction in consumption of the minimum extension of a given gate onto the field isolation region, and improved control and predictability during the trimming process, than is otherwise possible.